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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/057,817
Filing Date: January 22, 2002
Appellant(s): MARINO, CHARLES F.

Spencer K. Warnick
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 25 April 2007 appealing from the Office action mailed 24 November 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Blomgren (US 5,935,198)

Flahie et al. (US 5,912,832)

Christensen et al. (US 5,612,710)

Allen et al. (US 5,838,387)

(9) Grounds of Rejection

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3– 6, 8, 10 – 13, and 15 – 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Blomgren (US 5,935,198).

Regarding independent claim 1, Blomgren discloses a pixel format where each pixel have 4 8-bit components (R, G, B, A) (column 1, lines 44 – 60) and blending or interpolating two objects together (column 5, line 60 – column 6, line 61), which reads on the claimed receiving a request for blending the at least two images, each image having a pixel format. Blomgren discloses the full-size multiplier may be divided into smaller sections which can operate independently for 8-bit multiplies, or together as one large multiplier for 32-bit multiplies and all four smaller pixel components can be interpolated simultaneously in a larger multiplier (column 13, lines 28 – 43), which reads on the claimed reconfiguring each blending unit multiplier to perform at least two operations per cycle. Blomgren discloses the full-size multiplier may be divided into smaller sections which can operate independently for 8-bit multiplies, or together as one large multiplier for 32-bit multiplies and all four smaller pixel components can be interpolated simultaneously in a larger multiplier (column 13, lines 28 – 43), which reads on the claimed bit slicing each multiplier according to the pixel format.

Regarding dependent claim 3, Blomgren discloses the full-size multiplier may be divided into smaller sections which can operate independently for 8-bit multiplies, or together as one large multiplier for 32-bit multiplies and all four smaller pixel components can be interpolated simultaneously in a larger multiplier (column 13, lines 28 – 43) and the operands accommodating a plurality of bits, such as 8-bits or 16-bits (column 6, lines 53 – 56), which reads on the claimed bit slicing each multiplier to accommodate a first bits/pixel parameter of the pixel format.

Regarding dependent claim 4, Blomgren discloses the full-size multiplier may be divided into smaller sections which can operate independently for 8-bit multiplies, or together as one large multiplier for 32-bit multiplies and all four smaller pixel components can be interpolated simultaneously in a larger multiplier (column 13, lines 28 – 43) and the operands accommodating a plurality of bits, such as 8-bits or 16-bits (column 6, lines 53 – 56), which reads on the claimed bit slicing each multiplier to accommodate a second bits/pixel parameter of the pixel format.

Regarding dependent claim 5, Blomgren discloses the full-size multiplier may be divided into smaller sections which can operate independently for 8-bit multiplies, or together as one large multiplier for 32-bit multiplies and all four smaller pixel components can be interpolated simultaneously in a larger multiplier (column 13, lines 28 – 43) and the operands accommodating a plurality of bits, such as 8-bits or 16-bits (column 6, lines 53 – 56) and where the first bit is the most significant bit, being the bit on the far left of the operands and the product (Figure 9), which reads on the claimed first bits/pixel parameter is a highest bits/pixel parameter of the pixel format.

Regarding dependent claim 6, Blomgren discloses the full-size multiplier may be divided into smaller sections which can operate independently for 8-bit multiplies, or together as one large multiplier for 32-bit multiplies and all four smaller pixel components can be interpolated simultaneously in a larger multiplier (column 13, lines 28 – 43), which reads on the claimed highest bits/pixel parameter is no higher than 8 bits/pixel and no les than 1 bit/pixel.

Regarding claims 8, 10, 13, and 15, claims 8, 10, 13, and 15 are similar in scope as to claims 1, 3, and 4, thus the rejections for claims 1, 3, and 4 hereinabove are applicable to claims 8, 10, 13, and 15. Blomgren discloses a processor unit and a memory graphics processor circuitry (claim 9).

Regarding dependent claim 11, Blomgren discloses the binary multipliers adapted for 3-D graphics calculations (column 1, lines 10 – 12), which reads on the claimed blending unit is part of a graphics engine.

Regarding dependent claim 16, claim 16 is similar in scope as to claim 11, thus the rejections for claim 11hereinabove is applicable to claim 16.

Regarding dependent claim 12, Blomgren discloses the interpolation instruction being used for a white fog effect (column 3, lines 19 – 53) and other color interpolation operation such as anti-aliasing, depth cueing, texture-map interpolation, alpha blending, fog, translucency, Phong shading and Gouraud shading (column 3, lines 58 – 65), which reads on the claimed graphics engine further comprises at least one of a raster operator, a color key operator, a pixel bit mask operator, a patter write mask operator and a pixel boundary modify write operator.

Regarding dependent claim 17, claim 17 is similar in scope as to claim 12, thus the rejections for claim 12 hereinabove is applicable to claim 17.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren (US 5,935,198) in view of Flahie et al. (US 5,912,832) and Christensen et al. (US 5,612,710).

Regarding dependent claim 7, Blomgren did not expressly disclose dividing an 8-bit x 8-bit multiplier to perform at least two operations per cycle. Flahie discloses dividing an 8-bit x 8-bit multiplier into four 4-bit by 4-bit multipliers. Christensen discloses multicolor pixel word is a 16-bit word including 4 sets of 4-bits, each set describing a color (claim 3). It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Blomgren's system by dividing an 8-bit x 8-bit multiplier into 4 sets of 4-bit x 4-bit multiplier to perform interpolation on a 16-bit word color value where each set represents a color or even to perform interpolation of any n-bit x n-bit multiplication operation in any size multiplier where n is greater than or equal to 1 and n is less than the size of the multiplier's dimensions. One would be motivated to do so because parallel interpolation significantly improves throughput and to be compatible to perform interpolation of any n-bit color format, such as a 4-bit color format.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren (US 5,935,198) in view of Allen et al. (US 5,838,387).

Regarding dependent claim 18, Blomgren did not expressly disclose a scalar in the graphics system. Allen discloses a video scaling engine for scaling video data (abstract). It would have been obvious for one of ordinary skill in the art at the time of the invention to modify Blomgren's system to include a scalar. One would be motivated to do so because scaling data to a desirable size can improve bandwidth in communication or change a level to the desired detail in rendering images.

(10) Response to Argument

Applicant's arguments with respect to claims 1, 3 – 8, 10 – 13, and 15 – 18 have been fully considered but they are not persuasive.

With respect to claims 1, 8, and 13, applicant argues Blomgren does not disclose "reconfiguring each blending unit multiplier . . . wherein the reconfiguring includes bit slicing each multiplier according to the pixel format." Applicant agrees that Blomgren discloses dividing a 32-bit multiplier into 4 independent 8-bit sections, but does not include reconfiguring the 32-bit multiplier by bit slicing according to the pixel format of an image. Applicant is putting limitations into the claim language that is not expressed in the claims. The claim states "according to the pixel format", not "according to the pixel format of an image". Blomgren teaches each pixel has three color components, red, green blue, and a fourth color component, alpha and that interpolation must be performed on the color components (column 13, lines 17 – 21). Blomgren realizes, at the time of his invention, that modern microprocessors operate on 32-

or 64-bits of data and color components are typically 8- or 16-bits in size (column 13, lines 28 and 29). Blomgren also realizes that parallel processing is faster than series processing (column 13, lines 17 – 27). Because of this, Blomgren takes a full-size multiplier and divides the multiplier into smaller sections which can operate independently for 8-bit multiplies and interpolate the four color components simultaneously in the full-size multiplier (column 13, lines 32 – 37). Therefore, Blomgren takes a 32-bit multiplier and dividing (reconfiguring) the 32-bit multiplier into four multipliers, specifically four 8-bit multipliers, wherein the 8-bit multiplier conforms to a pixel format. Blomgren also takes a 64-bit multiplier and dividing (reconfiguring) the 64-bit multiplier into four 16-bit multipliers, wherein the 16-bit multiplier conforms to a pixel format.

Applicant argues that Blomgren does not disclose "bit slicing a same multiplier according to different pixel formats". Applicant's claimed invention states, "reconfiguring each blending unit multiplier to perform at least two operations per multiplier per cycle, wherein the reconfiguring includes bit slicing each multiplier according to the pixel format. Blomgren teaches this limitation as stated above. However, since Blomgren realizes modern technology, at the time of his invention, operates on 32- or 64-bits of data, using 32- or 64-bit multipliers with 8- or 16-bits size color components (column 13, lines 28 – 42), Blomgren divides the 32- or 64-bit multipliers into four 8- or 16-bit multipliers, respectively, according to pixel formats of 8- or 16- bit color components, respectively. Blomgren also realizes that parallel processing is faster than series processing (column 13, lines 17 – 27) and performs four parallel multiplier processes after dividing the 32- or 64-bit multipliers into four 8- or 16-bit multipliers, respectively, according to pixel formats of 8- or 16- bit color components, respectively.

Applicant states that, "in Blomgren, the 'smaller sections' (col. 13, line 33) within a multiplier are 'independent', and fixed, and can only be added 'together as one large multiplier' (col. 13, lines 34-35)". Blomgren cites on column 13, lines 32 – 37, "The full-size multiplier may be divided into smaller sections which can operate independently for 8-bit multipliers, or together as one large multiplier for 32-bit multiplies. Thus all four smaller pixel components can be interpolated simultaneously in a larger multiplier." Blomgren teaches a functionality of dividing a 32-bit multiplier into four independent 8-bit multipliers to perform interpolations of four color components simultaneously, parallel, or at the same time.

Examiner believes that dividing a 32-bit multiplier into four smaller sections for parallel processing of interpolations of 8-bit color components reads on the applicant claimed invention of reconfiguring a multiplier according to pixel format of an image.

Applicant argues that Blomgren does not disclose "blending the at least two images". Blomgren discloses a 32-bit multiplier being divided into four smaller sections to interpolate 8-bit color components at the same time (column 13, lines 17 – 42). Blomgren also discloses other interpolations, such as white fog may be superimposed over an object to give the illusion of a mist or fog between the viewer and the object (column 3, lines 22 – 25) and an example of blending using interpolation to produce a fog or translucency effect would be taking a blue triangle that has a color represented by $(RGBA)_B$ which is constant over an entire polygon (column 3, lines 27 – 30) and blending with a white fog represented by $(RGBA)_W$ (column 3, lines 39 and 40) and using the blending factor F that is calculated by the A value of the white fog (column 3, lines 40 and 41) to interpolate each of the color components of the blue triangle and

the white fog (column 3, lines 43 – 45). The blue triangle represents an image and the white fog represents another image (Figure 2).

Claim 7 stands and falls together with claim 1.

Claim 18 stands and falls together with claim 13.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Jeffrey J. Chow

Conferees:

Ulka Chauhan (SPE)

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER

Kee Tung (SPE)